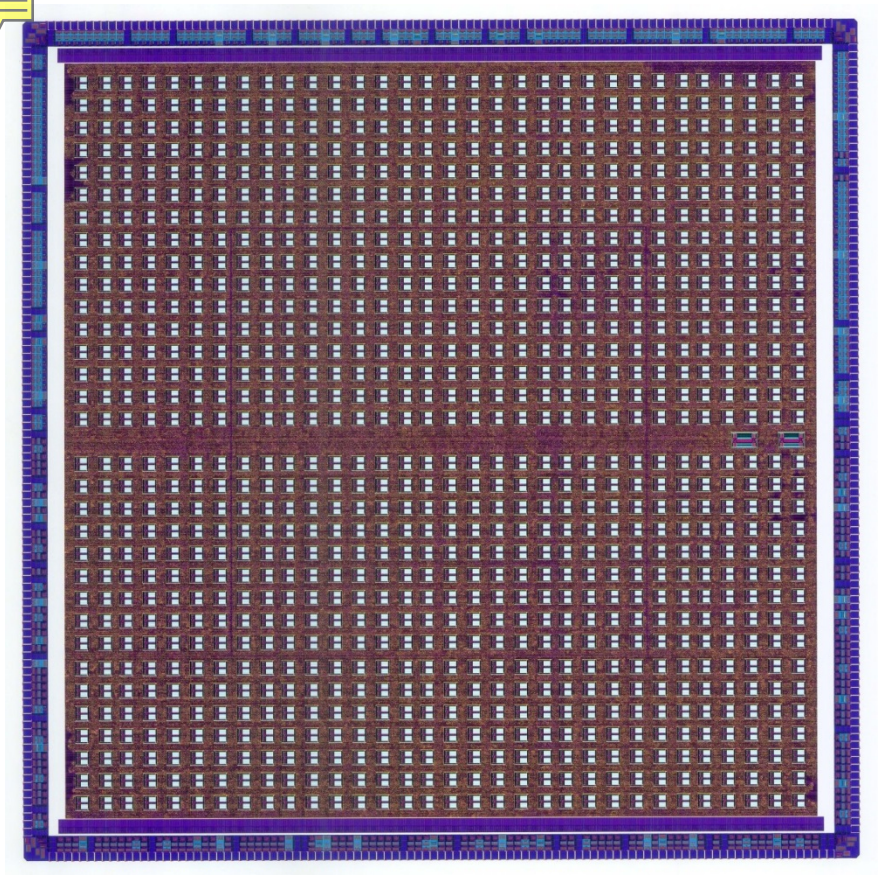
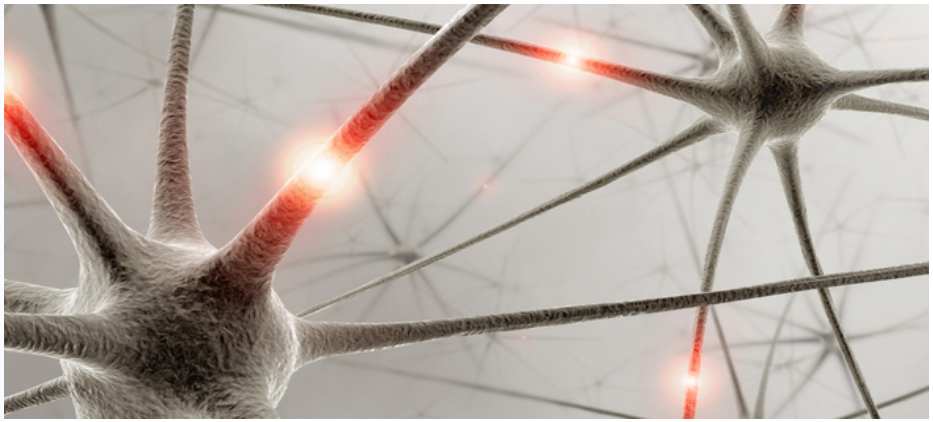


NEUROMEM
A ZISC ARCHITECTURE NEUROMORPHIC CHIP AVAILABLE TODAY!

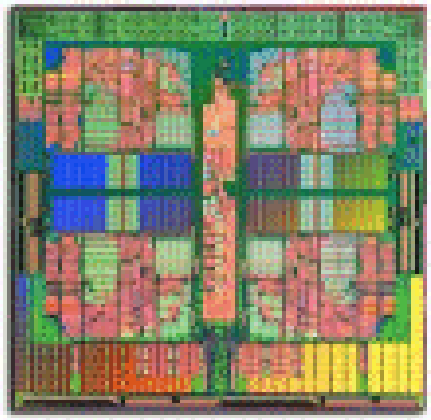


NATIVELY NEUROMORPHIC ARCHITECTURE WITH NO INSTRUCTION SET FOR LEARNING/RECOGNITION

The NeuroMem computing alternative

Today's common platforms

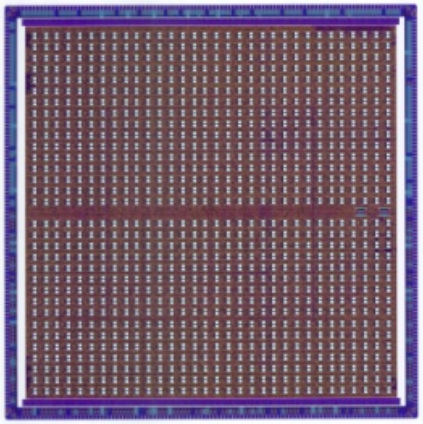
A multicore processor surrounded by DMA and SDRAM controllers; >1 GHz, >10 W



- Multi-core processors
- Memory misery bottleneck
- Limited by the Amdahl's law
- High frequencies (GHz), Power demanding (10W)
- Complex programming

The NeuroMem concept

Neuromorphic memory with 1024 identical cells; <16 Mhz, <0.5 W

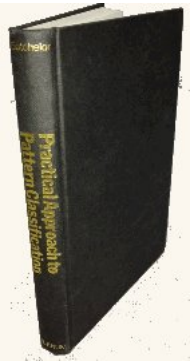


- Memory and processing logic combined in a same cell
- Identical cells working in parallel
- Fixed number of I/Os independent of the number of cells
- Zero Instruction Set Computing architecture
- less than 1 M$ development cost
- 130 nm 8 Metal layers 8x8 mm dies size

The 8 pillars of neuromorphic Pantheon

- **Broadcast Mode :** query/stimulus is broadcasted to all the neurons of a "context group" simultaneously
- **Deterministic search time:** does not increase with the scaling up of the network
- **Winner takes all:** Inhibit the weak responders autonomously in the same deterministic time
- **Uncertain response:** when there is multiple/conflicting neurons responding or "lesser quality" (degenerated) neurons spiking.
- **Unknown response:** Enable the dynamic addition of new knowledge
- **Back propagation of error:** Self & parallel inhibition of erroneous spiking neurons, no software involved
- **No fetch and decode of program instruction:** Software is definitively contrary to the biological model, else it's simulation, not neuromorphic…
- **Beyond biology:** Fast upload download enabling knowledge proliferation (some dream of it).

The merger of two old, but still in-fashion concepts



Non-linear classifier

***1974**, Compound classifier invented by Bruce Batchelor*

***1982** - Restricted Coulomb Energy classifier, derived by Leon Cooper (Nobel prize for supraconductivity)*

Hardwired parallel architecture

***1984** - CERN's UA1 experiment lead by Nobel prize winner Carlo Rubbia*

Guy Paillet DataSud Systems design a parallel architecture (60 CPU's/Memory on same VME bus)

Big Data before time

250 Gigabytes/second

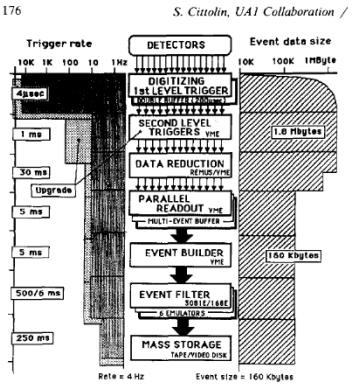


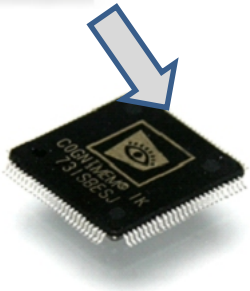
Fig. 2. The data acquisition stages.

***1993** - ZISC (Zero Instruction Set Computer with 36 and later 78 neurons)*

designed by IBM France and Guy Paillet

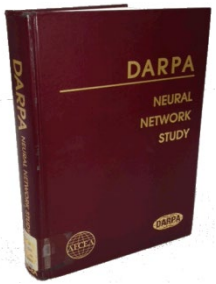
***2009** - CM1K (Cognitive Memory with 1024 neurons)*

designed by Anne Menendez and Guy Paillet



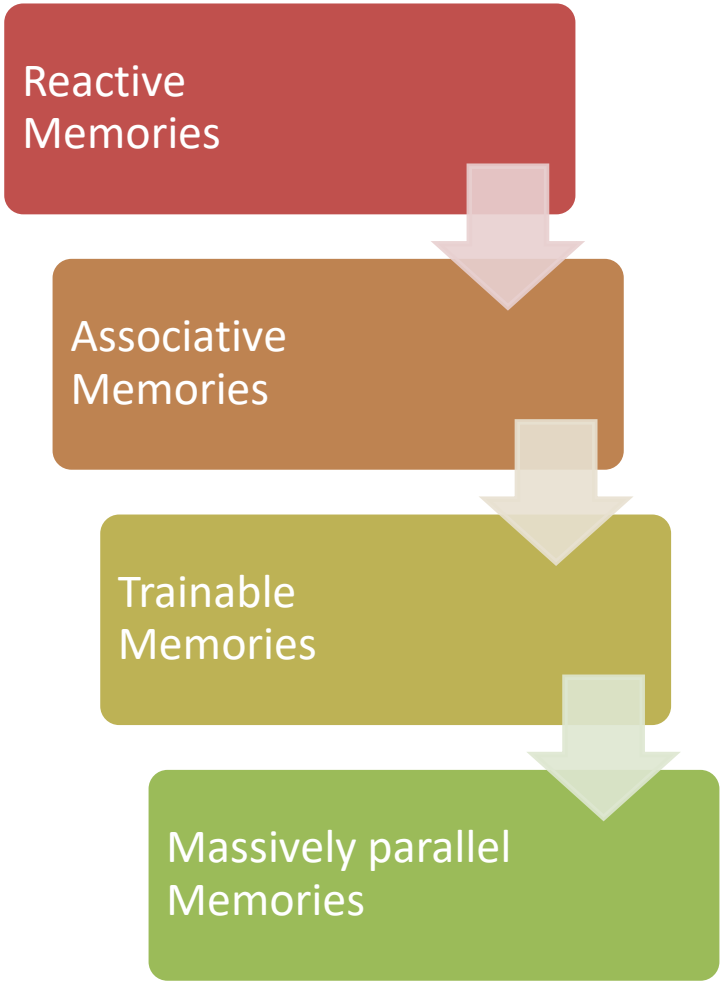
***1988** – DARPA Neural Network Study*

"The technology is not mature for widespread practical applications, since computer simulation are the primary methods of implementation."

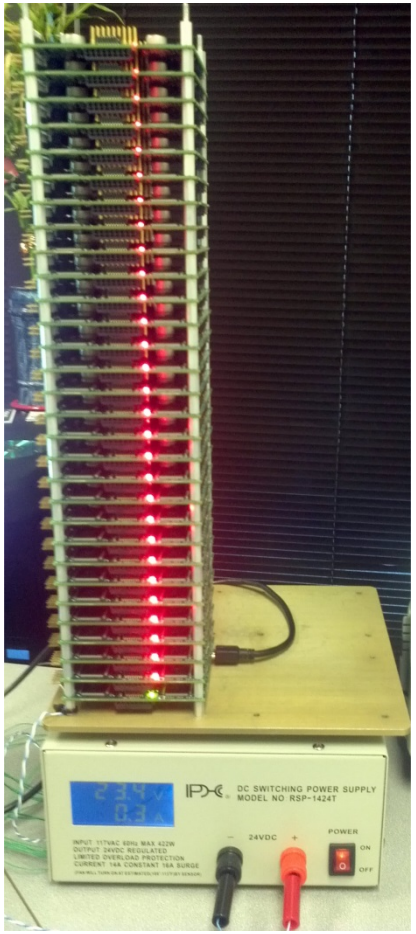


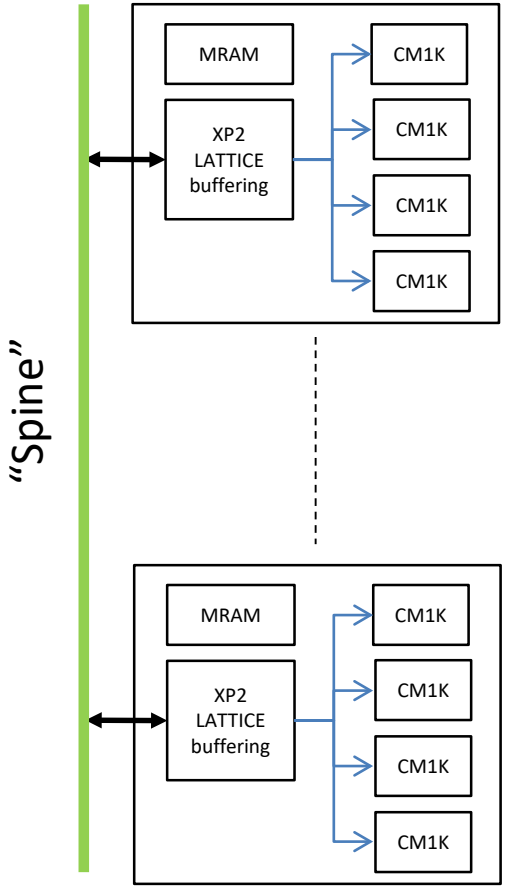
The NeuroMem Innovation

- **Reactive Memories:**
  - Deliver answers voluntarily when an input data matches their content. Instead of having a CPU screen sequentially what every memory 'knows', the memories volunteer their response in an orderly manner.
- **Associative Memories**
  - React not only when an input data matches their content, but also when it is similar "enough". This feature extends the usage model to a **non linear classifier.**
- **Trainable memories**
  - Know when an input data represents novelty. Can learn/add new models in real-time. If applicable, the memory cells recognizing the new example erroneously correct their influence field autonomously . This feature extends the usage model to a **trainable neural network.**
- **Massively parallel memories**
  - Implement a natively parallel architecture which allows the sizing of any bank of cognitive memories WITHOUT impacting the I/O counts nor the existing interfaces to external hosts. The memories connected in parallel are operated at low frequency and therefore require low-power.



A stack of 100,000 neurons fully operational



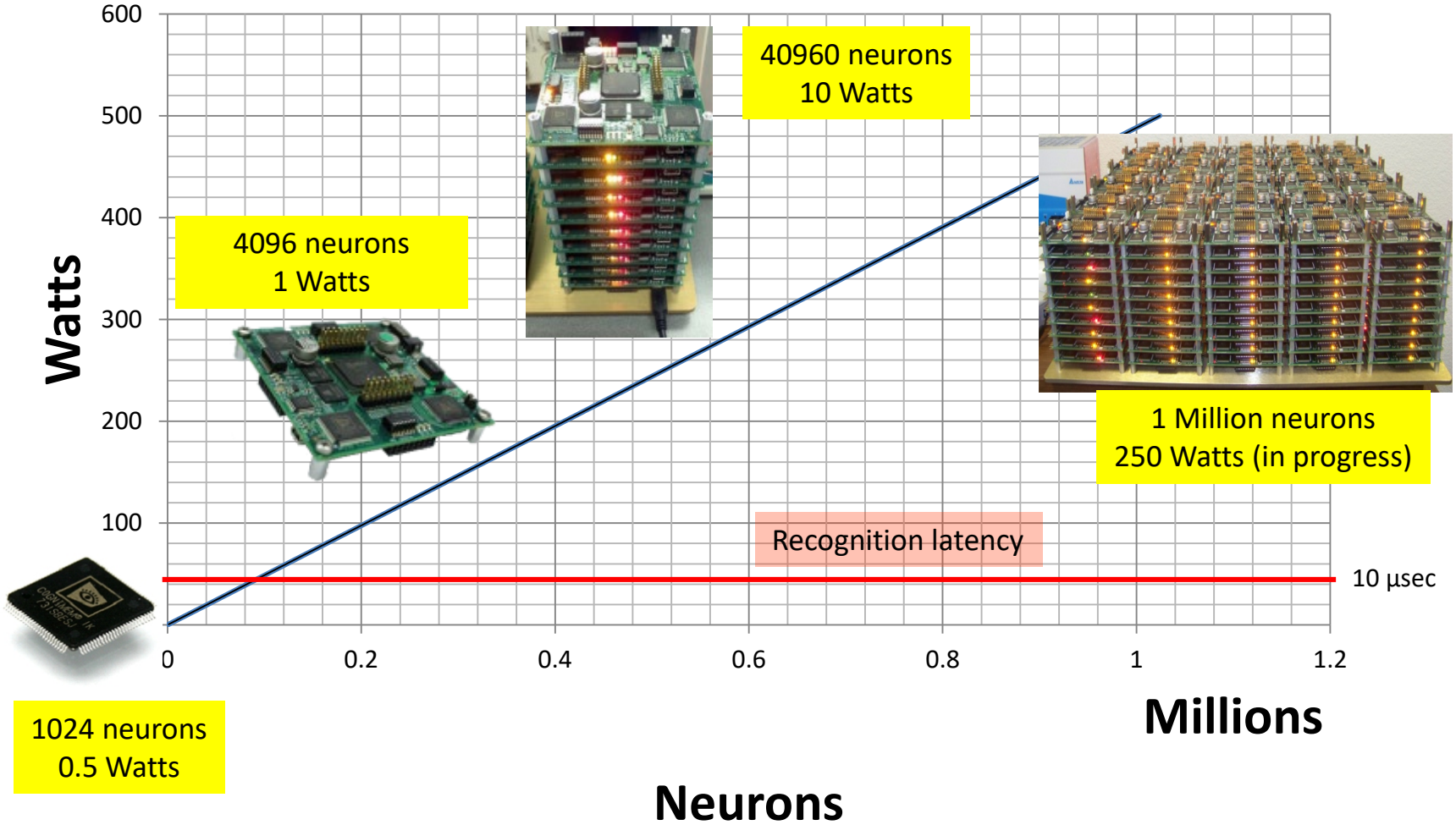


UP TO 25 NeuroMem Boards
409,600 operations per clock cycle @ 10 MHz
Total ~4 Tera Ops/sec
25 Watts

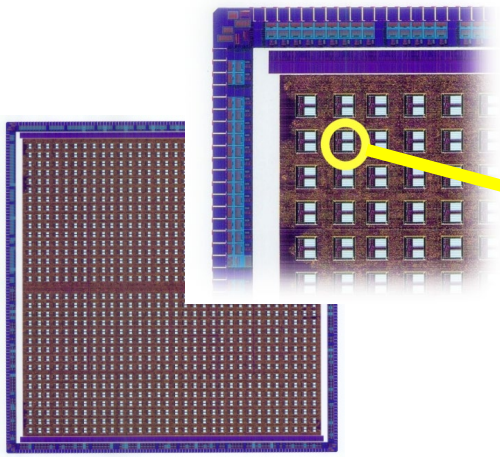
NEXT STEP

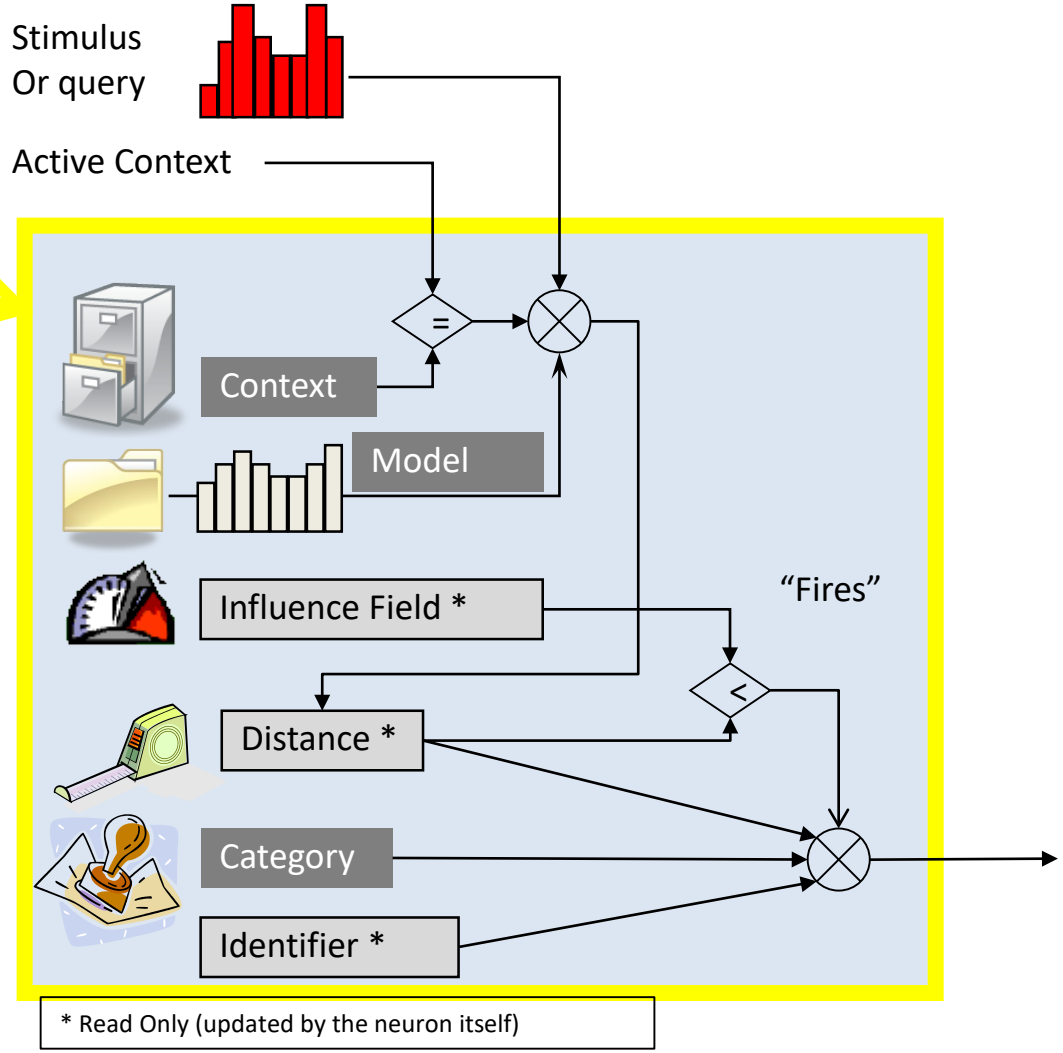
Reduce to a single chip in 2014

Demonstrated high Scalability



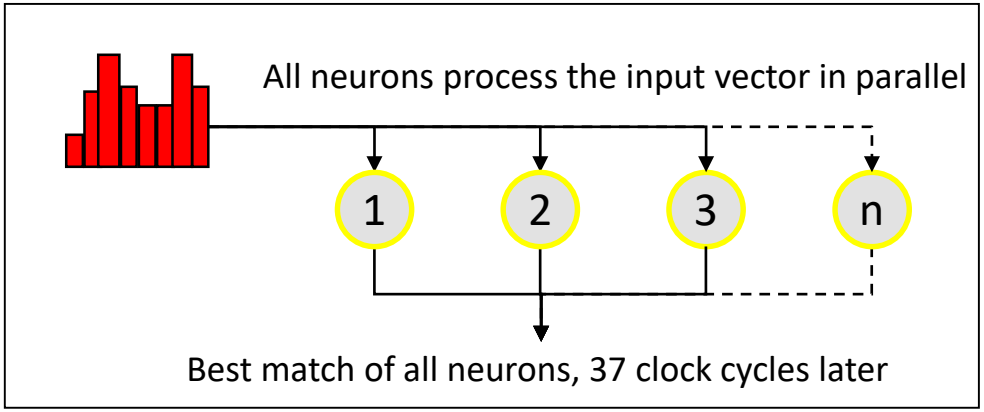
CM1K neuron architecture?





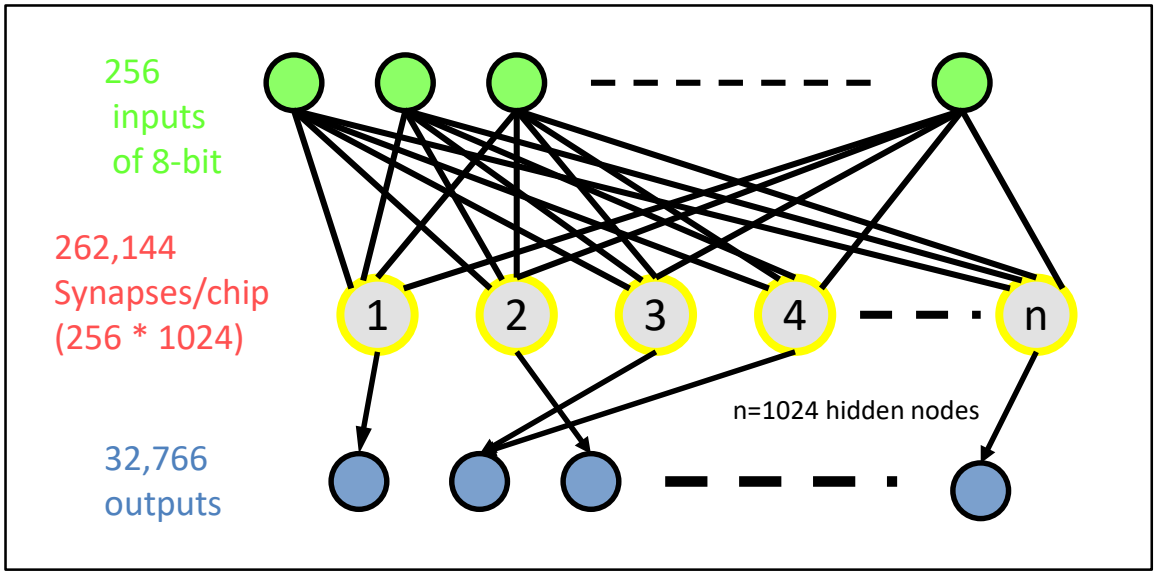
A CM1K neuron react (spike) which when incoming pattern is "similar" to its "learned" a memory. Similarity domain is adapted by excitation/inhibition during the teaching process. CM1K neurons are also able to make unsupervised leaning (e.g. clustering, etc…)

The CM1K neural network



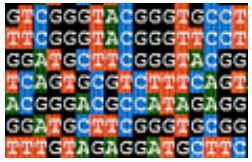
A neural network is a bank of neurons operating in parallel and interacting together to learn autonomously and recognize so that the **winner-takes-all.** All neurons have the same behavior and execute the instructions in parallel with no need for a controller or supervisor

CM1K seen as a 3-layer network



<u>Functions performed</u>:

- Identification
- Classification
- Clustering
- Anomaly Detection
- Novelty Detection

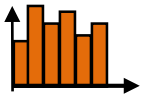


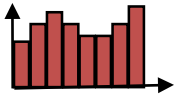
Text, DNA sequences

From Data to Insight…

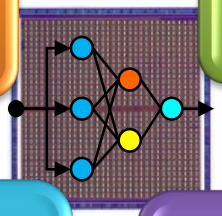
Audio, Voice, sensor signal

A signature or feature **vector** is extracted from a data source to model a given **context** of the data





The **vector** is broadcasted to all the **neurons** in parallel



The **neurons** knowledgeable about the selected **context** evaluate their similarity to the **vector**

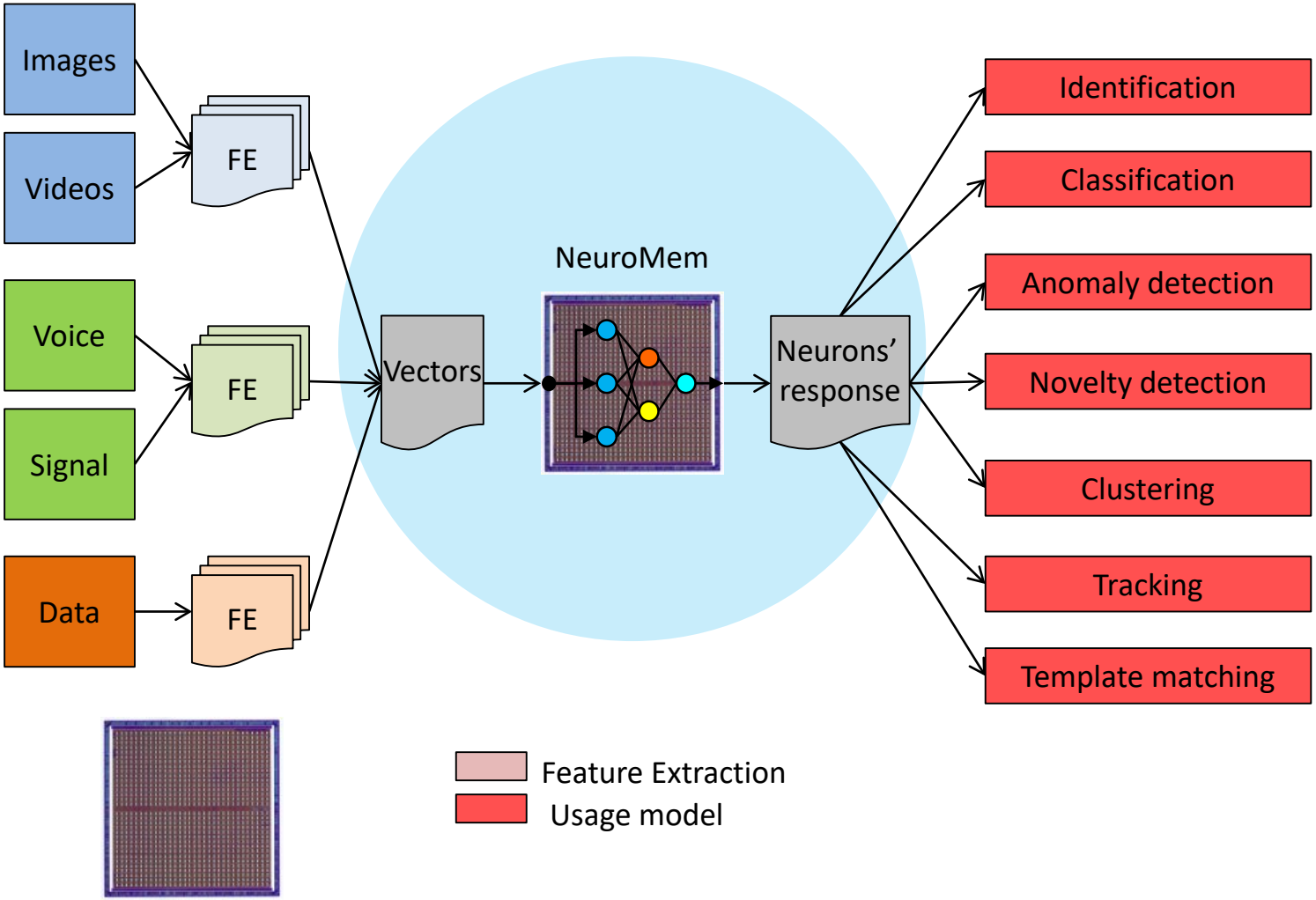
The "firing" **neurons** autonomously queue what they know about the vector in decreasing order of similarity

Their responses can be read AS IS or formatted into a new **vector** assigned to a different **context**

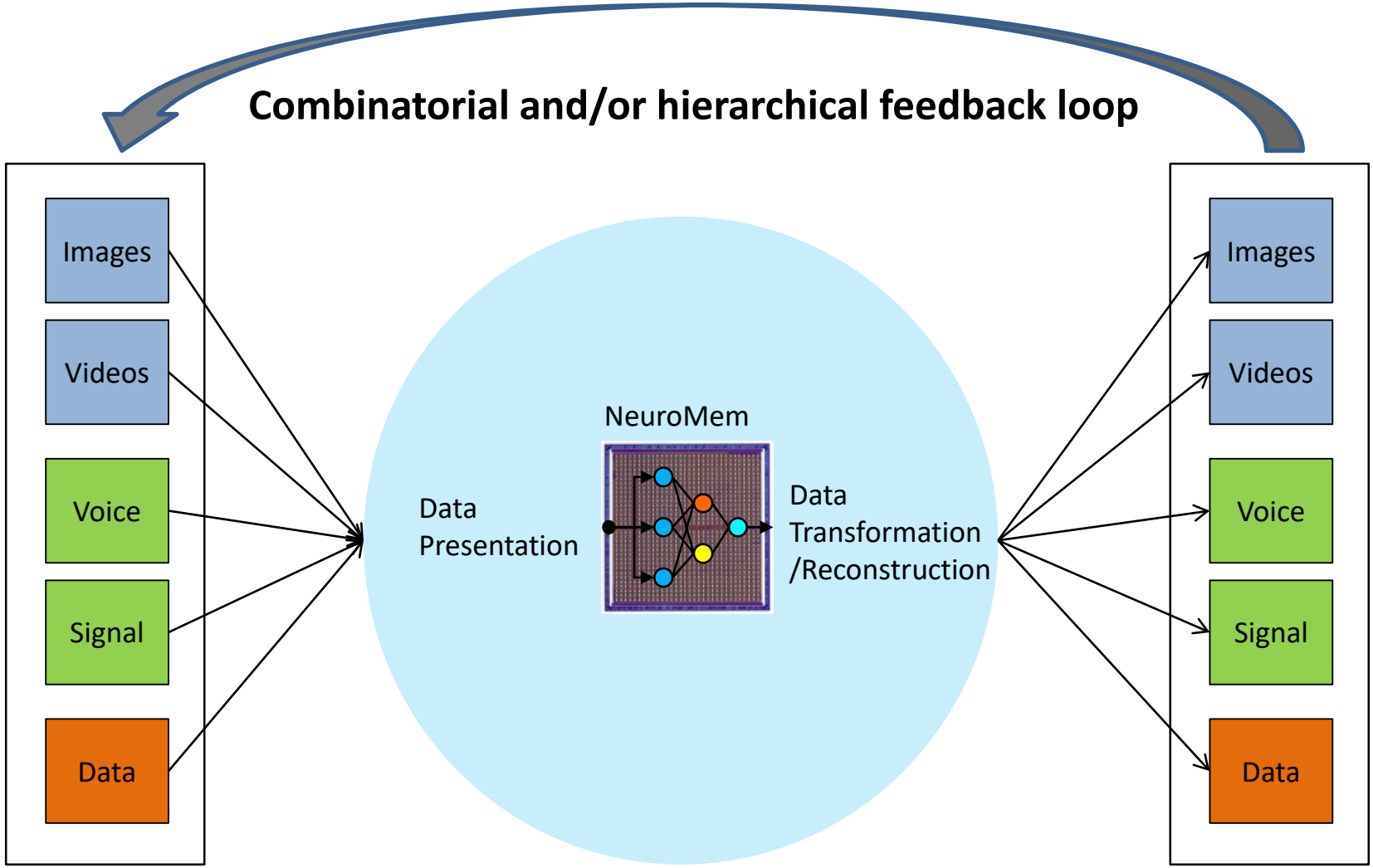
Videos

Images

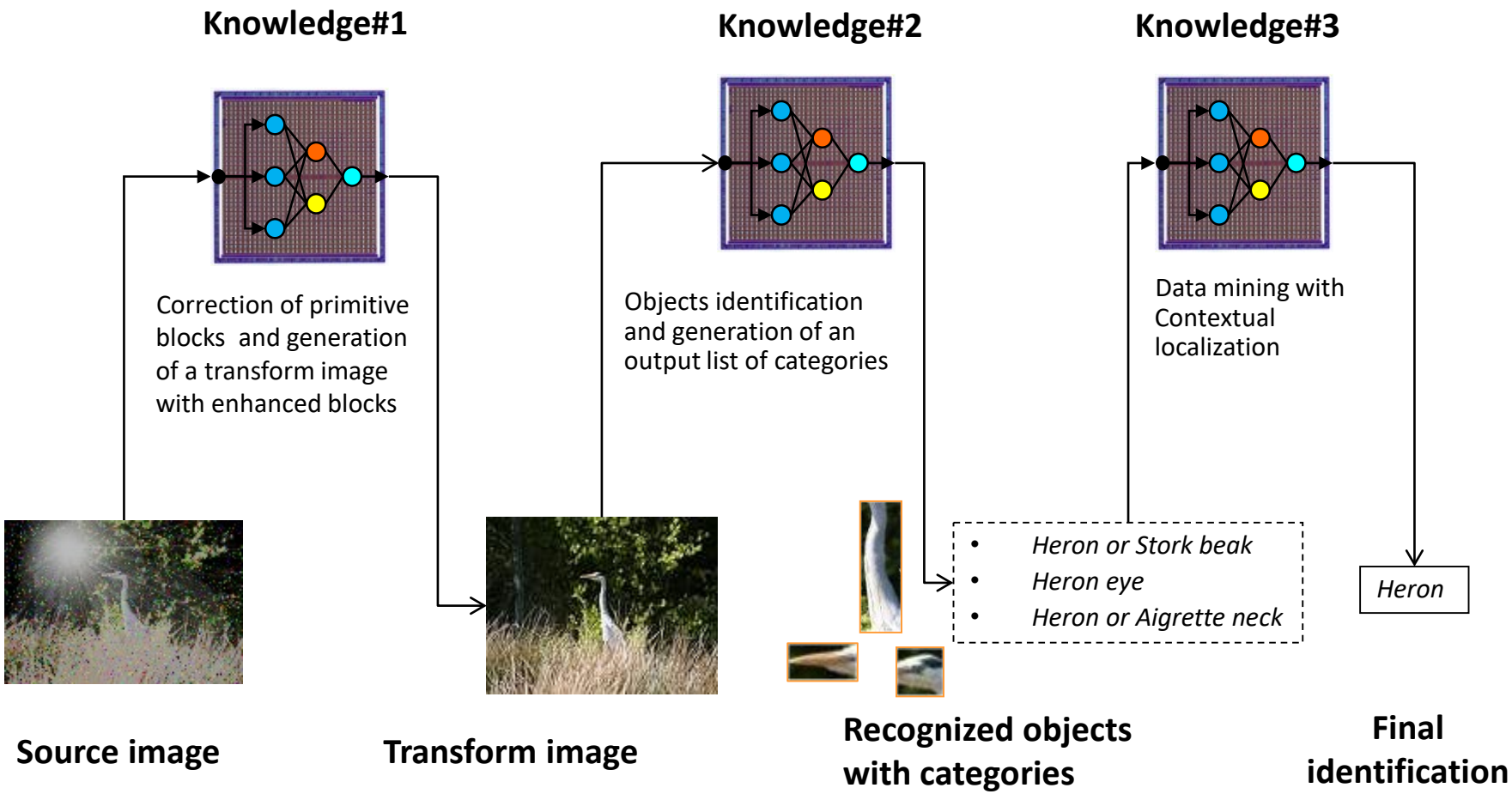
Usage Models, Level1



Usage Models, Level2



Ex1: Hierarchical decision making



Applications

- A companion processor to off-load the Van Neumann machines from pattern recognition tasks
- Cognitive Sensing
  - Convert sensor signals into insight data at the source and in real-time, selective transmission
- Cognitive storage
  - In storage search engines , scalable content access memory banks, intrinsic de-duplication, no need for indexing
- Cognitive networking
  - Match content of high speed data stream in real-time, selective pull data forward or exclusion

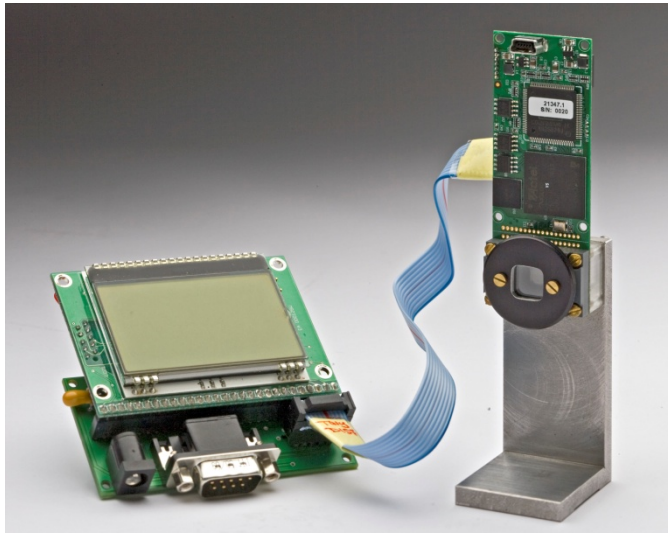
Engineering Diploma of the ENSPS

Master IRIV Nanophotonics

Thibaud MAGOUROUX

University year 2010

« DEVELOPMENT OF A MINIATURISED WAVEFRONT SENSOR BASED ON A SILICON NEURAL NETWORK »



01/03/2010 – 31/08/2010

Supervisors

Marc Eichhorn

Alexander Pichler

Already on the market

RoadNarrows Robotics
ROBOTICS AND INTELLIGENT SYSTEMS

CogniBoost™

CogniBoost™ offers an affordable, low-power, fast, pattern recognition module ideal for control applications, robotics, vision, & data mining.

Features:

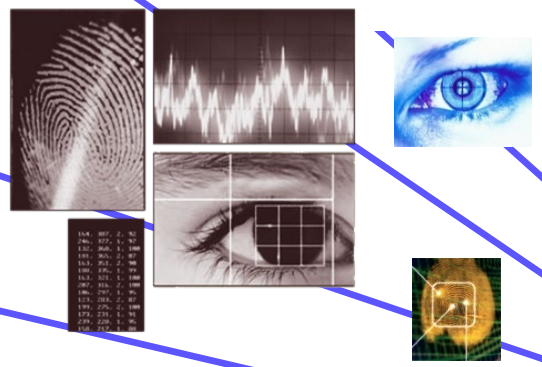
- Powerful embedded NeuroMem chip.
- USB interface provides both power and data interface to host.
- Standard USB driver support for Linux, Windows (FTDI) for USB to Serial COM.
- On-board non-volatile memory to store trained pattern categories & configuration.
- Binary or ASCII communications mode for different applications.
- Simple Microchip PIC managing protocol, neuron storage, and communications.
- Open protocol, free source code, & python examples for host applications.
- Supported by RoboRealm™ software under Windows.
- Ideal for embedded applications.

www.roadnarrows-store.com/products/think/cognitive-systems.html

Big Artificial Brain

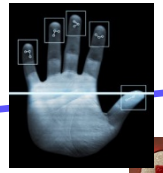
from the computer to the 'brainputer'

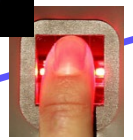
Artificial Intelligence and true parallel computing embedded system for ultra fast data base analysis by pattern matching

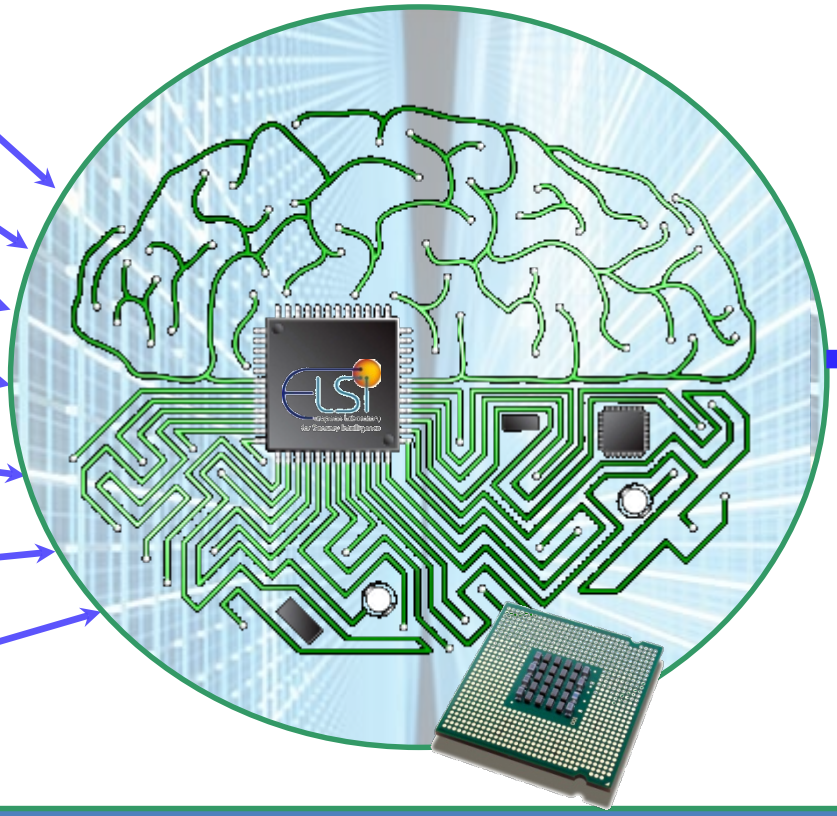


Biometric Data

DNA – fingerprint – iris – voice







Identification

Goal : 10^6 decision cells in parallel

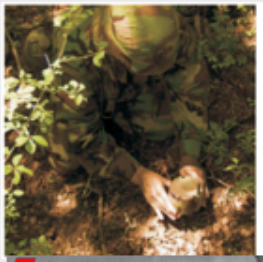
Droppable and disposable Miniature Visual Event Detector (in progress)

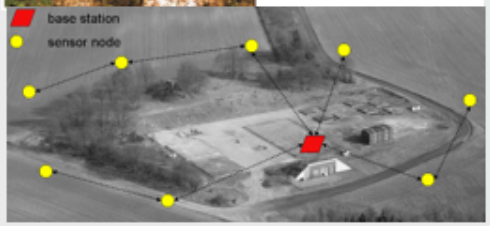
ATC/ELSI Team

MVED : Miniature Visual Event Detector
GENERIC USE CASES 2/3

AI on silicon could increase the performances of the sensors and the safety of our troupes, patrols, infrastructures.

➢**Increasing the number of MVED virtual experts**





- An intelligent camera could learn and track automatically a designed vehicle from node to node.
- The knowledge: a car signature … could be transferred to the other cameras at different sensitive points of the town.
- An intelligent camera could be trained to recognize ambulances and or vehicles of friendly forces.

8/14

Near Sensor Pattern Recognition