V1KU

Hardware reference manual

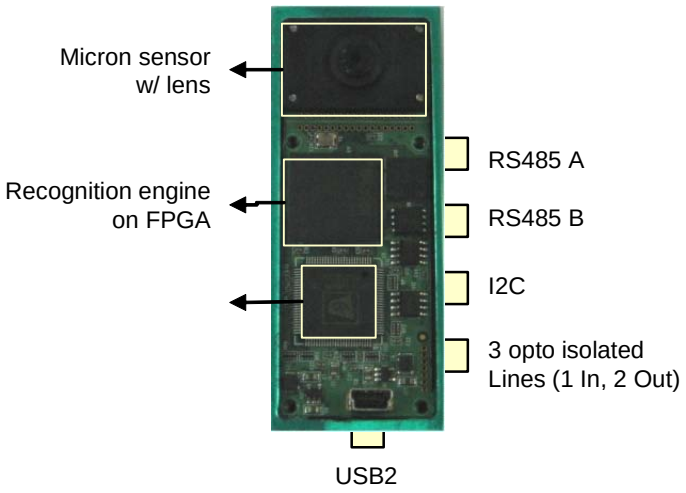

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Table of Contents

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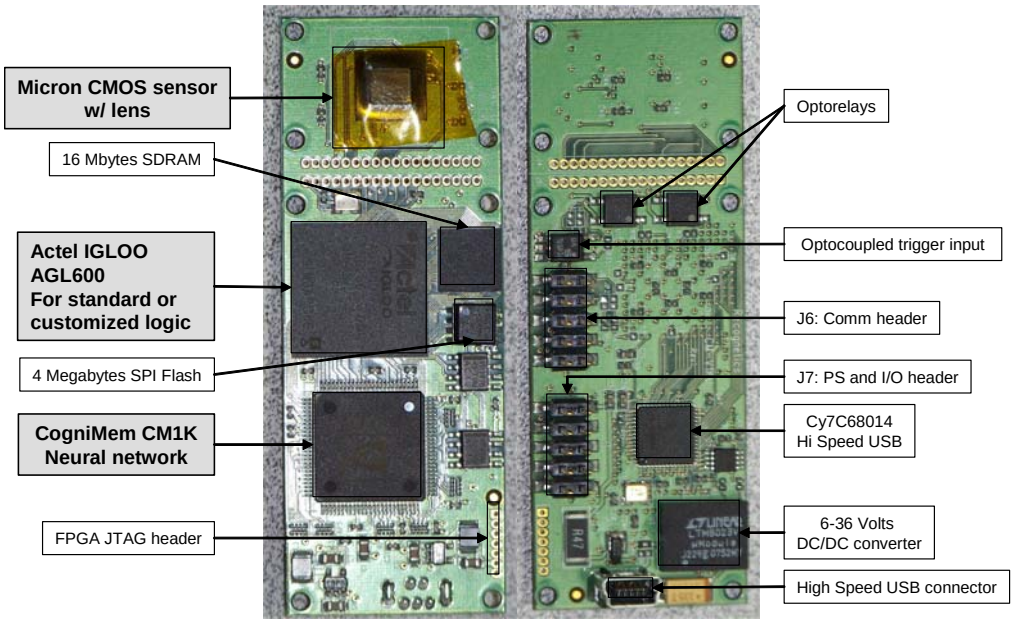
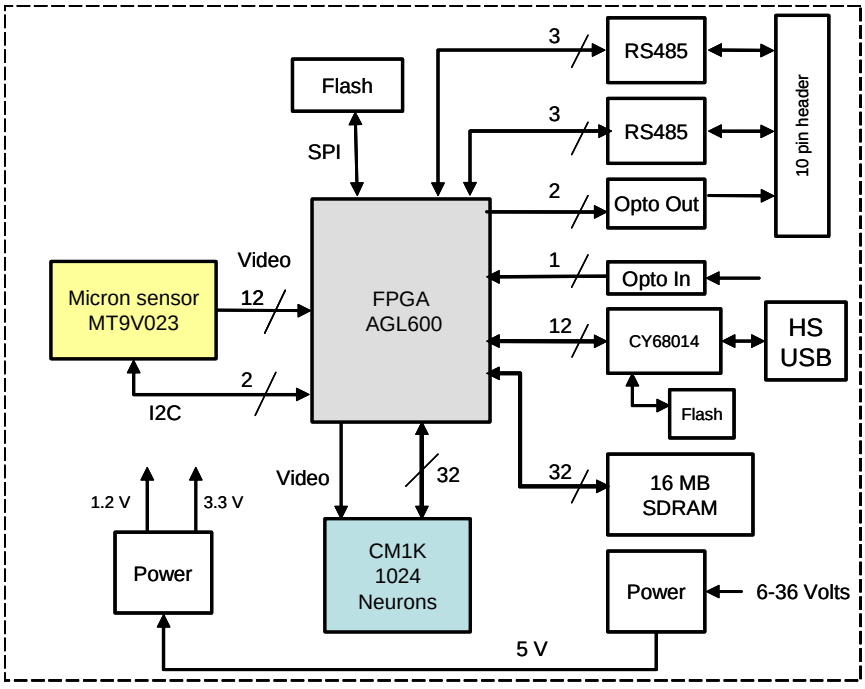
INTRODUCTION

V1KU is an evaluation module for the CogniMem technology applied to video and image recognition. The board features a CogniMem chip with 1024 neurons, a high quality Aptina monochrome video sensor, a reconfigurable Actel Field Programmable Gate Array (FPGA), 16 MB of SDRAM, 4 MB of Flash memory, one high-speed USB2 port, two RS485 ports, 2 opto relays, and one opto-isolated input line.



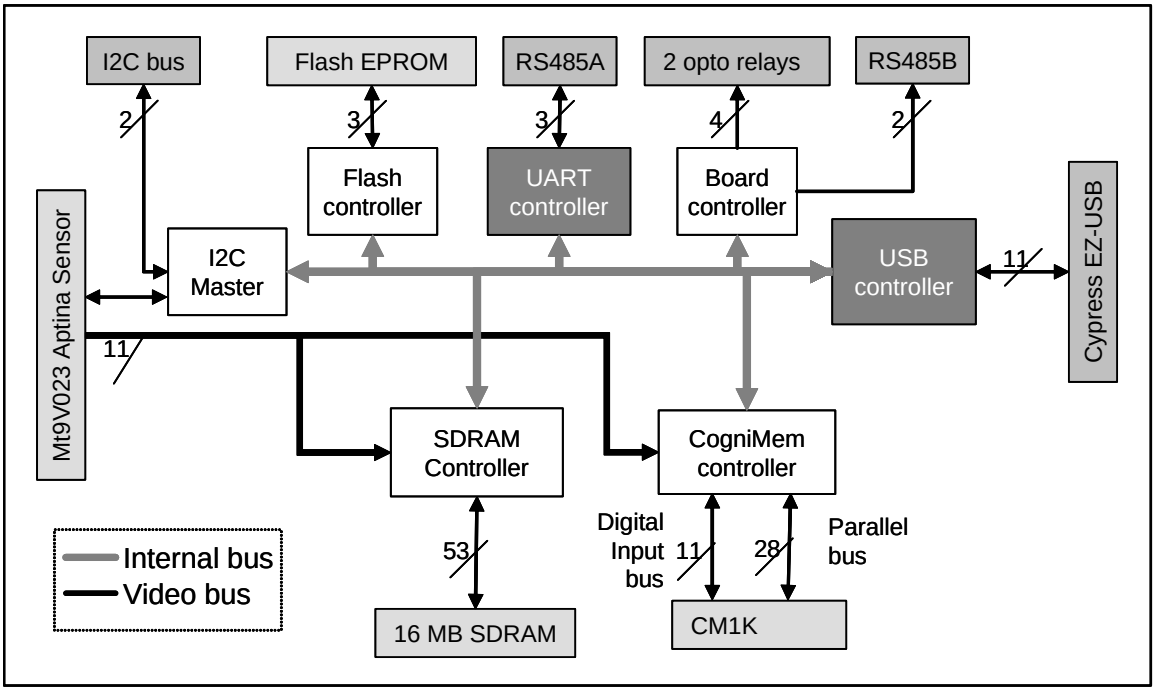
The CogniMem CM1K chip can learn and recognize pixel data coming directly from the Micron sensor or previously manipulated in the FPGA to produce a feature vector. In the former case, the feature vector is automatically extracted by the CM1K chip from a region of interest defined by the user. The FPGA can also consolidate and format the response of the neural network for transmission to the outside world. The SRAM is partially used to store the memory frame but can also hold user data.



Default factory programming:

V1KU is delivered with an FPGA programmed with the components presented in the diagram below.

Its simple recognition engine recognizes a region of interest 60 times per second. The region can be as small as 16x16 and large as the full video frame. The reported category is the one of the neuron with the best match.



A Software Development Kit is available for Windows developers and interfaces with the board through its USB or RS485A port.

An FPGA Development Kit is also available and includes the Verilog source code of the default FPGA firmware.

SPECIFICATIONS

Aptina MT9V022 video sensor

Monochrome, Progressive scan (color will follow)
752x480 pixels at 60 frames per second
Global shutter, Automatic exposure control (AEC), Automatic gain correction (AGC)
External trigger input
I2C sensor control

Lens (default)

60 degrees horizontal field of view angle
M7 (7 mm thread)
Adjustable to 10 mm horizontal Field of view (8 mm distance) to infinity

CogniMem CM1K chip

1024 silicon neurons working in parallel
Classify vectors of up to 256 bytes
Up to 16382 categories
Category readout in 36 clock cycles per firing neuron (i.e. 3 microsecond)
Radial Basis Function (Restricted Coulomb Energy) or K-Nearest neighbor classifier
Real time self-adaptive model generator

FPGA hosting recognition and decision logic

Actel IGLOO FPGA 600 (600,000 gates)
Default factory settings: CogniSight for Object Recognition (refer to the CogniSight engine manual)

Communication and I/O buses

USB 2.0 High Speed (up to 480 Mbps)
2 RS485 serial output (up to 921,400 baud- 115240 Standards)
Two opto-isolated relay output lines (<500 mA @60V)
One opto-isolated relay input line (<500 mA @60V)
I2C serial interface (up to-400 kbits)

Flash memory

2048 pages of 264 bytes. SPI access.

SDRAM

Micron MT48LC16M16A2. Synchronous DRAM 256Mb: 16 M x16bit SDRAM with SPI interface

Cypress USB chip

The Cypress Semiconductor Cypress CY7C68013A_8 USB Microcontroller chip supports the high bandwidth offered by the USB 2.0.

CONNECTIVITY AND I/OS

Connectors

J6 pins	Signal	Description
1	RS485B+	RS485 Channel B data+
2	I2C_SCK	I2C Clock
3	RS485A+	RS485 Channel A data+
4	I2C_SDA	I2C_Data
5	GND	GND power
6	Opto In	Opto In anode
7	RS485B-	RS485 Channel B data-
8	RS485A-	RS485 Channel A data-
9	Power	6-36 VDC power
10	Opto In	Opto in cathode
J7 pins		
1	VDC IN	6-36 VDC power
2	VDC IN	6-36 VDC power
3	RELAY(0)-0	Relay(0) output line 0
4	RELAY(0)-1	Relay(0) output line 1
5	RELAY(1)-0	Relay(1) output line 0
6	RELAY(1)-1	Relay(1) output line 1
7	OPTOIN-0	Opto In anode
8	OPTOIN-1	Opto in cathode
9	GND	GND power
10	GND	GND power

Power supply

V1KU can be powered between 6 and 36 VDC. The recommended power is 6 Volts. Typical consumption is 750 mW.

The power can be supplied through the USB port or through an external supply depending on the configuration of jumper J1.
- USB: solder bridge between pins 3 and 4 of J1 (factory default)
- External: solder bridge between pins 1 and 2 of J1

Both bridges can be soldered, BUT in this case, pay attention NOT to connect an external power supply if V1KU is connected to a host via its USB connector.

RS485 serial ports

The V1KU board features two pairs of bi-directional serial lines RS485A and RS485B supporting up to 20 Mbits and compatible with Profibus.

At factory settings, the FPGA implements the simple USB protocol described in a following chapter.

USB Communication

V1KU features an Easy USB chip from Cypress (Cypress CY7C68013A -56LFXC) with an embedded 8051 processor. It can be programmed with the Keil Development Tools (http://www.keil.com).

It offers the following features:
• An integrated, high-performance CPU based on the industry-standard 8051 processor.
• A soft (RAM-based) architecture that allows unlimited configuration and upgrades.
• Full USB throughput. USB devices that use EZ-USB chips are not limited by number of endpoints, buffer sizes, or transfer speeds.
• Automatic handling of most of the USB protocol, which simplifies code and accelerates the USB learning curve.

The chip is connected to the IGLOO FPGA via an 8-bit data bus and also via its I2C serial lines. In the default configuration, the Cypress chip uses its I2C lines only to interface with a Microchip Flash memory (8 kbytes) holding its configuration settings. Its slave address is #A0.

At factory settings, the FPGA implements the simple USB protocol described in a following chapter.

I2C lines

Two lines on the jumper J6 are reserved for I2C serial communication. They are disabled by default to ensure that the internal I2C communication between the Cypress chip and the Micron sensor are not disrupted.

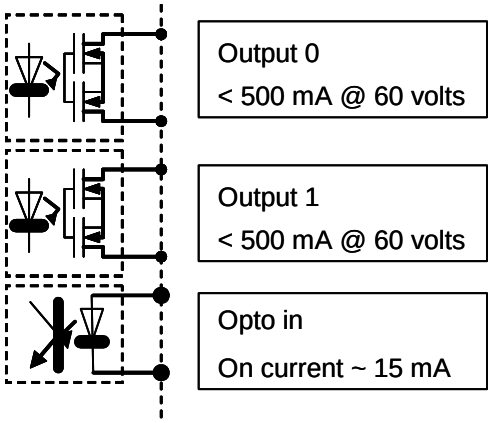
You can enable the communication between V1KU and two external I2C lines by configuring the jumper JP2 as follows:
SCK enable: solder bridge between pins 1 and 2 of JP2
SDA enable: solder bridge between pins 3 and 4 of JP2

Opto-isolated relay outputs

Two opto isolated relay outputs can drive up to 60 volts 500 mA continuously or up to 1500 mA during 100 milliseconds pulse.

Trigger Input

A current flow (25 mA max) can be applied between the anode and cathode of the Opto_In line.



JTAG

The IGLOO FPGA is programmable through a JTAG (J2) and FlashPro programmer from Actel.

The Libero IDE development software is downloadable from Actel web site at www.actel.com. The default CogniSight engine loaded in the FPGA at factory settings is available in Verilog code in the V1KU_SDK_FPGA package.

ACCESSORIES AND OPTIONS

Back enclosure with single connector and splitted wires

Description	Color Coded cable
RS485 Channel B data+	*Not yet available*
RS485 Channel A data+	*Not yet available*
RS485 Channel B data-	*Not yet available*
RS485 Channel A data-	*Not yet available*
6-36 VDC power	*Not yet available*
Relay output 0 cathode	*Not yet available*
Relay output 0 anode	*Not yet available*
Relay output 1 anode	*Not yet available*
Relay output 1 cathode	*Not yet available*
Opto In anode	*Not yet available*
Opto in cathode	*Not yet available*
GND power	*Not yet available*

Faceplates and lens selection

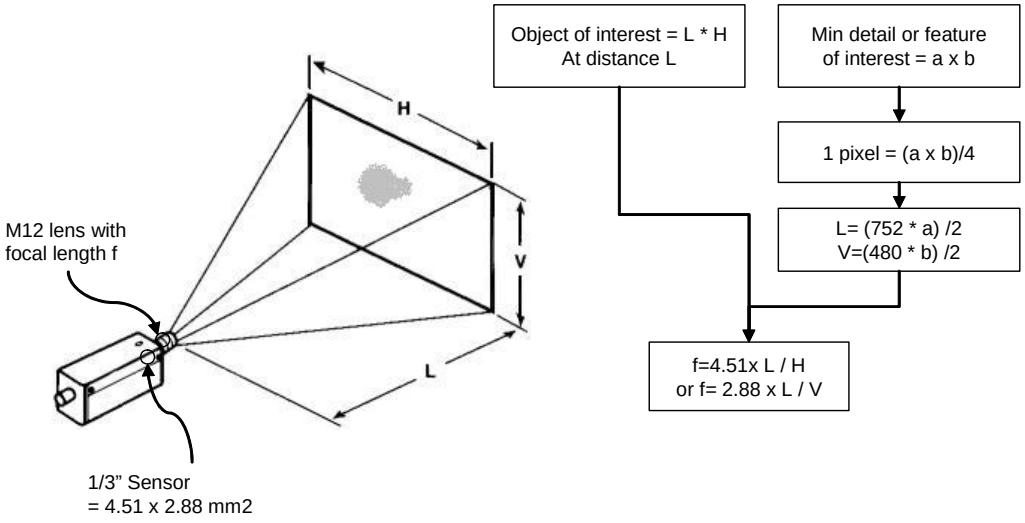
V1KU comes with an M7 lens with a 6mm focal length. Optionally V1KU can be mounted with a faceplate compatible with M12 lenses.

How to choose a lens?

If your object of interest is contained in a Field of View (FOV) with the dimensions HxV when placed at a distance L from the sensor, then one pixel represents H/752 x V/480 mm^2.

The minimum details to detect in the field of view should be at least equal to 2x2 pixels. From there you can find calculate the parameters H, V and also L, if applicable.

The focal length of the lens is then equal to f=4.51x L / H or f= 2.88 x L / V. The multiplication factors derive from the fact that the Aptina sensor mounted on the V1KU has a 1/3" optical format, that is 4.51 x 2.88 mm^2.



DEFAULT COMMUNICATION PROTOCOL

At factory settings, the various components of the V1KU board are easily accessible through the Register Transfer Level (RTL) protocol programmed on the FPGA and described below. This protocol is interpreted by both the USB controller and RS485 controllers.

Packet protocol description

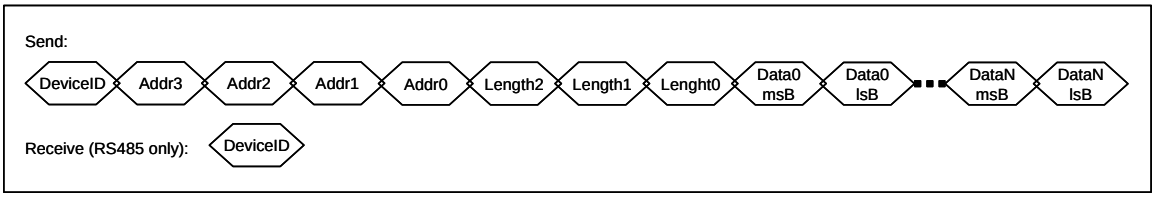
All the components of the V1KU board can be accessed through the following read/write protocol. Data access can be made for single words or series of words.

1 byte	4 bytes	3 bytes	N words
DeviceID	Address bit[31]= Read(0)/Write(1) bit[30-24]= controllerID* bit[23-0]=registerID**	Datalength Length of data read or written by the transaction expressed in bytes	Data If L is the value transmitted as Datalength, N must be equal to L÷2.

*Each component of the board is associated to a controller.
**Each controller accesses its proprietary registers.

	ControllerID	RW registers	R only	W only
CogniMem controller	0x01	22	2	1
I/O controller	0x02	2	6	0
Flash controller	0x03	0	1	7
I2C master controller	0x04	n/a		
SDRAM controller	0x05	2	0	0
Communication controller	0x0A	2	0	0

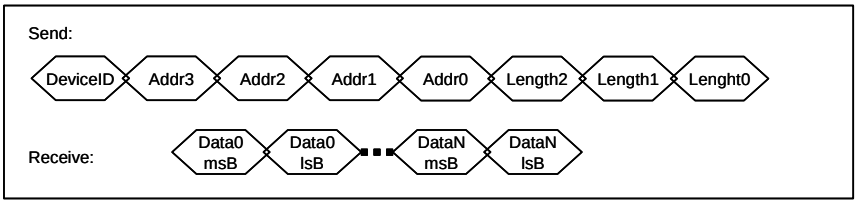
Write command (Addr31=1)



Example:

Write 0x8000 to the CogniMem Context register	0x01	0x0100000B	0x001	0x0800
Returns	0x01			

Read command (Addr31=0)



Example:

Read board's serial number	0x01	0x82000023	0x001
returns	0x40		

RS485 specification

V1KU supports the above protocol on its RS485 port A at 921,600 baud with Data bit=8, Stop bit=1, Parity= None, Handshake=None.

USB specifications

The USB bulk transfers of the V1KU board are handled by the Cypress EZ_USB chip (CY7C68014, 56-pin model). Packets from host to V1KU must be sent to the end point EP2_OUT. Packets from the device to the host are received on the end point EP6_IN.

The EZ_USB chip features an CPU 8051 and internal RAM. The CPU implements the high-level USB protocol by servicing host requests over the control endpoint, but can also be used for general-purpose operations.

Drivers and USB development tools can be downloaded from the Cypress web site. Cypress includes an evaluation version of the 8051 Keil Software Tools in the USB 2.0 development kit.