

The V1KU\_FPGA Development Kit provides FPGA developers with IP cores interfacing with the different components of the V1KU board including the CogniMem CM1K chip and the Micron/Aptina CMOS sensor but also the memory and I/O chips. Using this SDK, FPGA programmers can greatly reduce their design costs and time to add new functionalities to the V1KU board and make it a high-speed and high performance image recognition sensor, yet embedded, miniature, low-cost and low power.

### Package contents

- Staple file
- IP core source code in Verilog
- Constraints file
- Pin assignment and attribute file

### IP core library

- USB controller (decode the packets received from the host over the USB end-points and broadcast them to the internal control and data bus)
- UART controller (decode the packets received from the host over the RS485 portA @ 921,600 bauds and broadcast them to the internal control and data bus)
- CogniSight controller (default version, acting as a pass-thru to the CM1K video recognition logic)
- CogniMem controller (access the neurons through their parallel bus)
- Sensor I2C master controller (read/write the registers of the Micron sensor and other device implementing the same I2C protocol)
- I/O controller (read hardware information, control opto-isolated lines settings, transmit the IsB of the last recognized category over the RS485 portB at 115,200 bauds)
- SDRAM controller (access a memory page, grab to and read frame from a memory page, read/write data in single or multiple burst)
- Flash controller (read/write data to page, read and execute, read and execute at reset)

### Requirements

- Libero IDE development software, free download from Actel web site
- FlashPro programmer available for USB or parallel port
- Custom JTAG adaptor to plug into J2 of the V1KU board (specification given in manual)

